

Low Power Reconfigurable Controllers for Wireless Sensor Network Nodes

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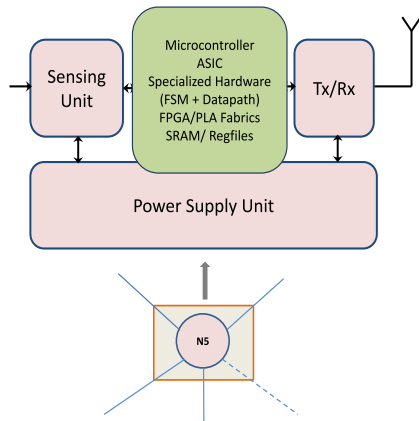


Outline

- 1 Introduction
- 2 Reconfigurable Microtasks
- 3 Flexible FSMs and Variable Precision Adders
- 4 Energy Efficiency and Cost of Flexibility
- 5 Conclusions

WSN Node Controllers: Functions and Constraints

Typical node with its controller



Functions

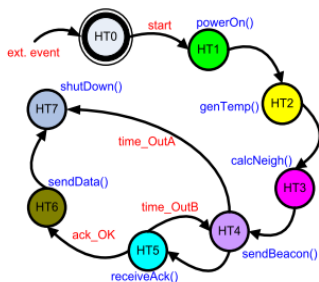
- Manage resources
- Interface with other units
- Perform computations, handle interrupts and events

Constraints

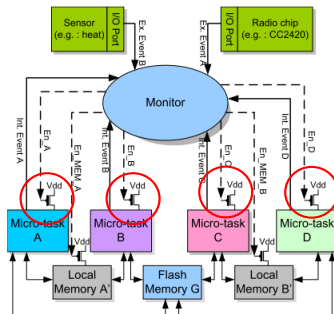
- Power and energy consumption
Autonomy and battery lifetimes
- Flexibility
Variable applications
Energy-aware protocol adaptations

Controllers Based on Microtasks

A design flow for generation of ULP WSN node architectures based on microtasking

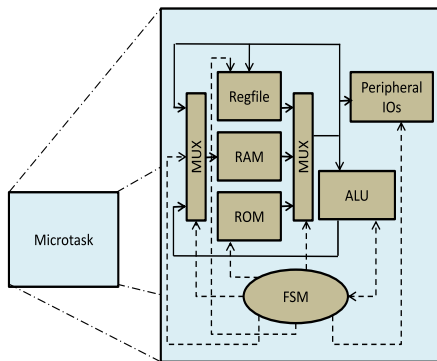


Task Flow Graph



System Level View of
Generated Architecture

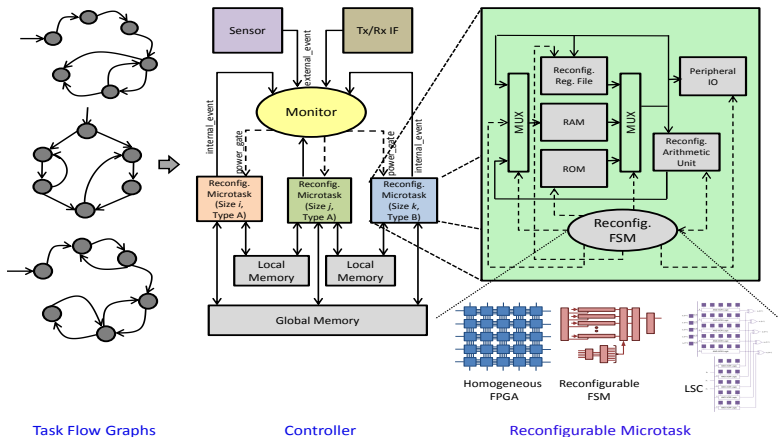
Microtask Architecture



- Based on a FSM + Datapath Model
- Datapath: ALU, Memory, IO Interfaces
- General in structure, but ASIC-like function results from FSM specific to task
- Task scheduling by a System Monitor

Reconfigurable Controller

A typical reconfigurable microtask-based controller



Task Flow Graphs

Controller

Reconfigurable Microtask

Opportunities for Power Gating

Shannon decomposition for power gating granularity

Next-state function

$$s_i(t+1) = f_i(x_0, x_1, \dots, x_{n-1}, s_0, s_1, \dots, s_{N-1})$$

$$s_i(t+1) = \sum_{k=0}^{2^{(n+N-K)}-1} m_k f_i(n(m_k), \dots, s_{N-1})_k$$

Example: $n = 3, N = 7, K = 6$

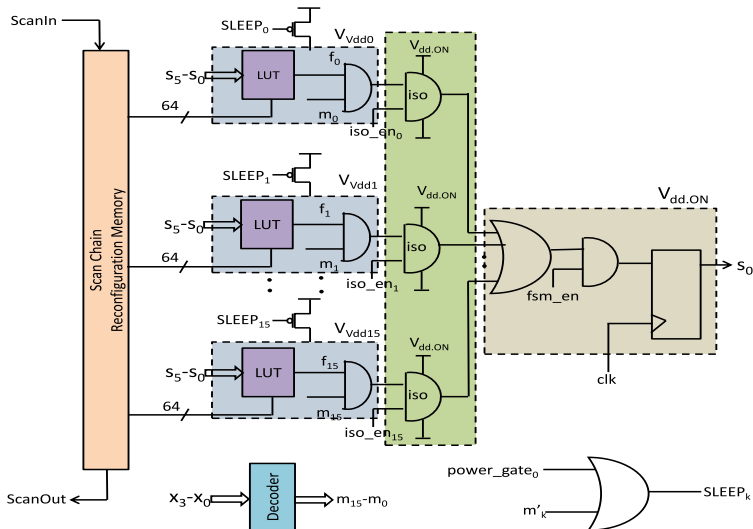
$$m_0 = x'_0 x'_1 x'_2 s'_0$$

$f_i(0, 0, 0, s_1, s_2, s_3, s_4, s_5, s_6)_0$ - implemented by K -LUT

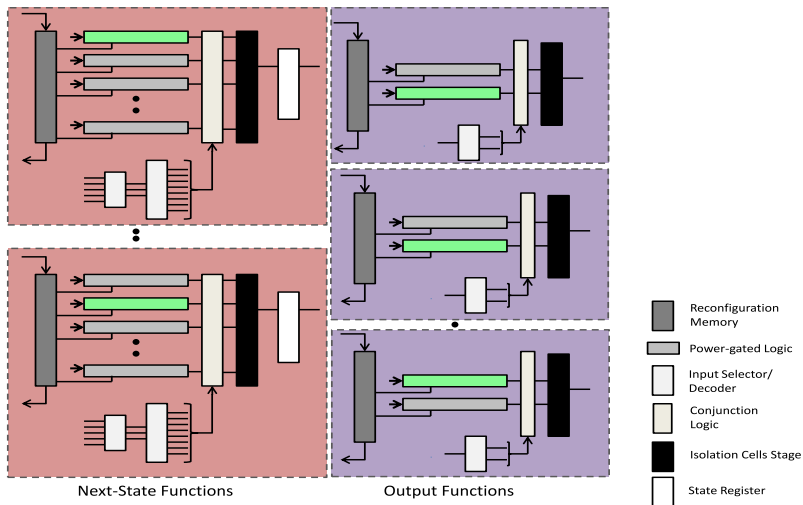
⇒ Determines size of K -LUT logic cluster for which power gating may be applied

Similarly for output functions

Power-Gated Reconfigurable FSMs

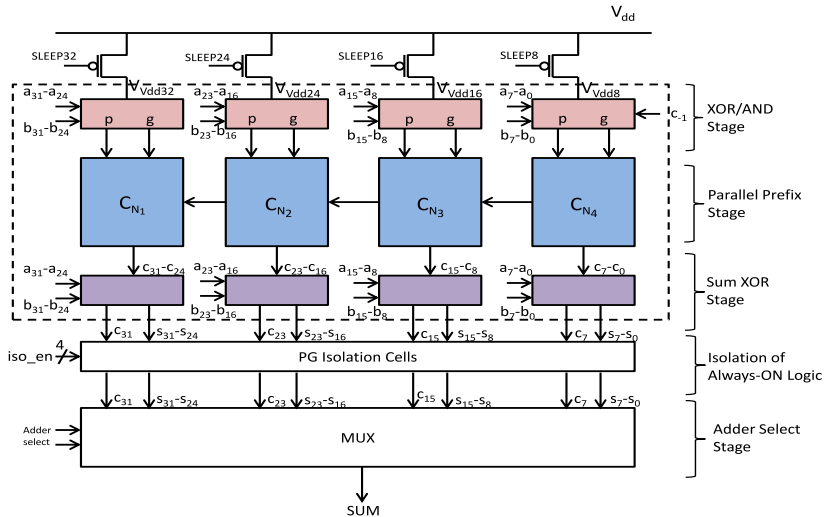


Overall Architecture



Power Gating in Adders

As applied to two adder structures: Brent-Kung and Kogge-Stones



Comparison between various realizations

Equivalent energy per instruction in three realizations of node controllers

Microtask	Equivalent Energy per Instruction (pJ/Inst.)					
	openMSP430		Reconfigurable Microtasks		16-bit Hardwired Microtasks	
	N_{inst}	E_{eei}	N_{states}	E_{eei}	N_{states}	E_{eei}
Crc8	30	163	71	31.60	71	8.1
receiveData	66	230	332	83.53	332	15.7
Crc16	27	170	73	41.27	73	9.3
firBasic	58	179	168	46.90	168	26.1

Comparison of areas of 16-bit hardwired and reconfigurable microtasks with an embedded FPGA and microcontroller

Microtask	Hardwired Microtask(μm^2)	Reconfigurable Microtask (μm^2)	eFPGA (μm^2) (217 CLBs)	openMSP-430(μm^2) ^a
Crc8	3097	140,522	1,076,871	22,141
receiveData	2858			
Crc16	3102			
firBasic	7164			

^aNo SRAM

Conclusions

- Explored reconfigurable architectures for FSMs and adders for flexible microtask-based controllers
 - Proposed scalable architectures for LUT-based FSMs
- Reconfigurable microtasks offer about $2\text{-}5\times$ better energy per operation compared to microcontroller at $5\times$ cost *w.r.t* hardwired microtasks
 - A typical WSN controller consists of 50 microtasks
- To explore further
 - Alternate reconfiguration mechanisms
 - Combinations of LSCs and power-gated FSMs

Thank you for your attention